REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold type.

> **Claims 1-11, 13-19, 21-26, and 28-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Johnson et al. (US 2003/0084253).**
>
> **Regarding Claims 1-2, Johnson discloses a computer system comprising: a cache (Figure 1) including cache lines to store data (lines 0-3 of data section 106), at least a portion of the data to be written to main memory (when a cache line is evicted, it is copied to or written to main memory, paragraph 006), and an eviction mechanism (state machine 116, Figure 1 and paragraph 0010) to evict data stored in one of the cache lines (cache line not accessed or changed may be preemptively evicted) based on validity state information (age bit in second logical state) associated with the data stored in the cache line, the eviction mechanism to send evicted data to the main memory (when a cache line is evicted, it is copied to main memory, paragraph 006).**

The applicant thanks the Examiner for the telephone interview on December 22, 2004. The applicant and the Examiner discussed the claims and the Johnson reference, as reflected in the remarks below.

Johnson does not disclose or suggest "an eviction mechanism to evict data stored in one of the cache lines based on validity state information that indicates the status of the data stored in respective portions of the cache line," as recited in amended claim 1.

Johnson states that, "[t]ypically, the minimum amount of memory that can be transferred between a cache and a next lower level of the memory hierarchy is called a line" (paragraph 0003). In Johnson, age-bits are used to "indicate whether lines in [a] cache may be stale" (paragraph 0017). In Johnson, "[a] single age-bit may be provided for each line in the cache, or a single age-bit may be provided for each index" (paragraph 0010), in which an index is a subset of an address that "designate[s] a set of lines within the cache" (paragraph 0014). Thus, Johnson discloses a system in which the age-bits are used to indicate whether one or more complete cache lines are stale. Johnson does not disclose or suggest that data are evicted "based on validity state information that indicates the status of the data stored in respective portions of the cache line," as recited in claim 1.

Claims 10 and 13 are patentable for at least similar reasons as claim 1.

Regarding Claim 18, Johnson discloses a computer apparatus comprising: a computer chipset comprising a cache memory to store write data sent from an input/ontput device (Figure 1) and a mechanism (state machine) to evict the write data from the cache memory when a set of predefined conditions are met (age bits in second logical state, paragraph 010). Since the system of Johnson is that of a common computer system, the system must inherently be connected to an input/output device given that a system such as this system is usually connected to a keyboard or mouse (input/output device). It is known that a user has the ability to create files through the use of a keyboard and mouse and such files could be the generated data that is stored in the cache.

Johnson does not disclose or suggest "a cache memory to store write data sent from an input/output device, the data being stored in the cache memory before being written to a main memory," as recited in amended claim 18. Although the system of Johnson could have an input/output device, Johnson does not disclose or suggest that the write data sent from the input/output device are stored in the cache memory before being written to a main memory. If the Examiner continues to regard that write data generated from input/output devices could be stored in a cache memory, the applicant would request that the Examiner provide a reference that discloses a cache memory storing write data sent from an input/output device, in which the data is stored in the cache memory before being written to a main memory.

Claim 22 is patentable for at least similar reasons as claim 18.

The dependent claims are patentable for at least the same reasons as the claims on which they depend.

Cancelled claims have been cancelled without prejudice. Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing attorney docket 10559-639001.

Respectfully submitted,

Date: 12/23/2004

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** See attached document certifying that Rex Huang has limited recognition to practice before the U.S. Patent and Trademark Office under 37 CFR § 10.9(b).*

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Expires: October 12, 2005

Harry I. Moatz
Director of Enrollment and Discipline